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RECEIVER SYSTEM ANALYSIS AND OPTIMIZATION

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systemIC, Inc.

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14. ABSTRACT

This project has advanced significantly the state of the art in analog/mixed-signal/radio frequency integrated circuit system design methodology and its supporting design automation technology. The new design methodology offers important improvements in system performance as well as in system design productivity. The novel analysis and simulation algorithms developed in this project have the potential to significantly impact performance of systems under Together, the methodology and design automation technology can help to reduce the non-recurring engineering costs and the cost-overruns that may arise in some USAF programs. The feasibility of both the methodology and the algorithms has been demonstrated. Efforts to integrate the technologies into existing design flows by major EDA vendors have, however, failed. Major EDA vendors seem to have little motivation to meet the unique requirements of the USAF. They also prefer not to enable a potentially disruptive technology that could rival their existing capabilities.

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1. Summary

The United States Air Force (USAF) requires the design of electronic systems of ever growing complexity. Due to performance, space, power consumption and reliability requirements, more analog, RF and digital functionality must be integrated into a single integrated circuit. The design of such complex and high-performance mixed-signal integrated circuits exceeds the capabilities of existing design methodologies and the electronic design automation (EDA) tools that support those methodologies. Shortcomings of the current methodologies and EDA tools include the inability to simultaneously design and analyze the analog, digital and RF parts of a design; system-level optimization for global goals such as power consumption; optimization of inter-cell impedance levels; simulation speed and accuracy. Efforts at overcoming these shortcomings have been limited to incremental improvements to 40-year-old circuit simulation technology and macromodeling. Neither has been particularly successful.

This project has attempted to address the above shortcomings by introducing a fundamentally different analysis engine. The engine, DesignAsyst™, was developed by systemIC, Inc. prior to the contract. This project focused on improving the DesignAsyst™ capability to address unique USAF requirements and demonstrate its capabilities on a design.

An AFRL MDREX receiver design on an IBM SiGe process was used to demonstrate the accuracy and capability of DesignAsyst™. We demonstrated that DesignAsyst™ is accurate and capable of analyzing the receiver for the required performance metrics: system noise figure, system gain, system linearity and output spectrum.

Although limited access to the system design team and to the digital part of the design limited our ability to optimize the system, we have identified several parts of the design that offer improvements in system performance.

A new design methodology for integrated RF circuits has been developed to address issues in macromodeling, inter-block impedance design and global optimization. Traditional design methodology calls for functional active blocks with their own passives as loads and matching elements to a pre-determined impedance such as 50 ohms. In addition, there are passive filters. The new methodology introduces a new hierarchy for RF circuit blocks that breaks the circuit into active units, or *mini-macros*, and passive units that combine impedance matching and filtering functionality and are inserted between the *mini-macros*. The new methodology allows designers to make best use of advanced silicon processes (scale, fast devices) while minimizing the disadvantages (low-Q passives, low transimpedance). A new abstract passive stage model was developed to support the new design methodology in DesignAsyst™. The new model supports *top-down* design of passive stages and is capable of comprehending the limitations of the particular process technology, i.e., the impact of parasitics on passive circuitry performance.

Several breakthrough analysis and design technologies were developed as part of the project. Most significantly, a transistor-level simulation algorithm compatible with the system level simulation algorithm was developed. This algorithm replaces the slow, unreliable, inaccurate and low-capacity co-simulation algorithms based on running a system-level simulator and a transistor-level simulation program simultaneously and synchronizing them at time intervals. Since the new capability allows the simulation of the entire system down to the transistor level, it also replaces bottom-up macromodels that are very costly to develop for each block and not always accurate.

2. Introduction

2.1 Background

The United States Air Force (USAF) requires the design of electronic systems of ever growing complexity. Due to performance, space, power consumption and reliability requirements, more analog, RF and digital functionality must be integrated into a single integrated circuit [1]. There have been several AFRL projects that aim to bring the advantages of integration to designs. In particular, the MDREX project has used IBM SiGe technology to achieve the exacting requirements of a phased-array radar on smaller form factors [2].

The design of such complex and high-performance mixed signal integrated circuits exceeds the capabilities of existing design methodologies and the electronic design automation (EDA) tools that support those methodologies. The MDREX program drove requirements for the DARPA NeoCAD program, which aimed to develop a new generation of EDA capabilities. The NeoCAD program was successful in advancing the state of the art in the automatic design and optimization of cell level RF and microwave designs including electromagnetic simulation [3]. Although cell-level design productivity gains were valuable, one of the findings of that effort was that much the advantage of integration is available only through system-level design and optimization. Some of the electromagnetic solver technology and cell-level design optimization technology developed under NeoCAD found their ways into commercial EDA solutions, but none of the system-level work did.

The traditional paradigm for the design of mixed-signal electronic systems is based on a mostly one-way divide-and-conquer strategy (Figure 1). An electronic system such as a radar receiver is first analyzed on a spreadsheet that uses intuitive formulae and the system designer's experience. The system designer decides on a system architecture. Very early on, a division is made between analog and digital mostly based on intuition and experience. This subdivision is often suboptimal. Specifications for the analog/RF sub-system are determined. The analog-RF sub-system, also known as the analog front-end, is further divided into components such as amplifiers, filters, mixers, oscillators, etc. Specifications for the components are then passed on to design teams. The digital and analog design teams are often separate and communicate little if at all. The interfaces between the components are at a pre-determined impedance (often 50 ohms) to facilitate an independent (one-way) design flow and make individual testing possible. These matching stages are cascaded in the system, leading to potential waste of area and performance (Figure 2). Each component is designed, manufactured and tested on the target technology. Several iterations may ensue depending on the performance of the components relative to the specifications initially allocated by the system designer. This is especially exacerbated by the fact that there are no process informed (parameterized) top-down macromodels for analog or RF components that can help the designer choose specifications that are feasible in the target process technology. If it turns out that the specifications for one (or more) of the components were unrealistic, the system design is updated, so all the components must

be redesigned. An important problem in redesign is that there are no top-down models for the passives that envelope the active devices in a component and perform loading, filtering and matching functions. The passives are manually crafted and must be redesigned from scratch with every iteration of the design. The lack of abstraction for passives also makes it more difficult to parameterize component macromodels because of the very large number of [seemingly] independent parameters that arise.

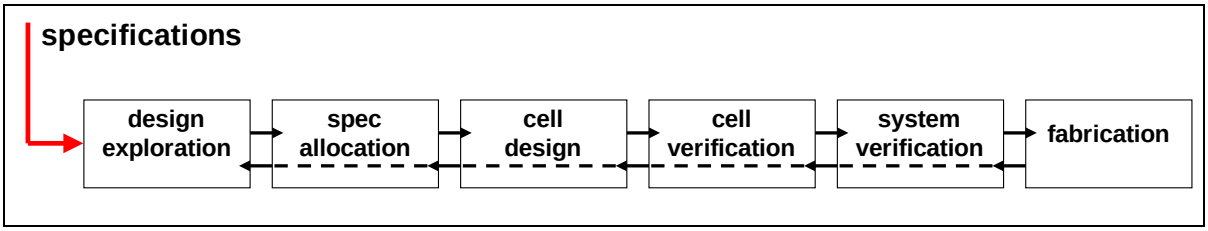

Figure 1. Communication Systems Design Methodology

Once components are mostly meeting specifications, verification of the entire system is attempted. It is often not possible to simulate the entire system at the transistor level; therefore macromodels are generated for each component, either from measurements or from circuit level simulations of the components. The analog/RF portion of the interconnected system is then simulated using these macromodels. Any problems detected by the simulations are then ironed out either at the component or system level. A mixed-signal simulation even using macromodels is often outside the capability of existing simulation tools. After this stage, the system is manufactured and tested. The tests often reveal problems with the design that were not revealed through simulations, such as spurs and system-level instability. The simulation problems are often due to oversimplifying assumptions in the macromodels, or unexpected interaction between the analog/RF and digital parts of the design. The problems are traced, spotted, and corrected at the component or system level. This entire process is long, resource intensive and expensive. It can take years and many manufacturing runs.

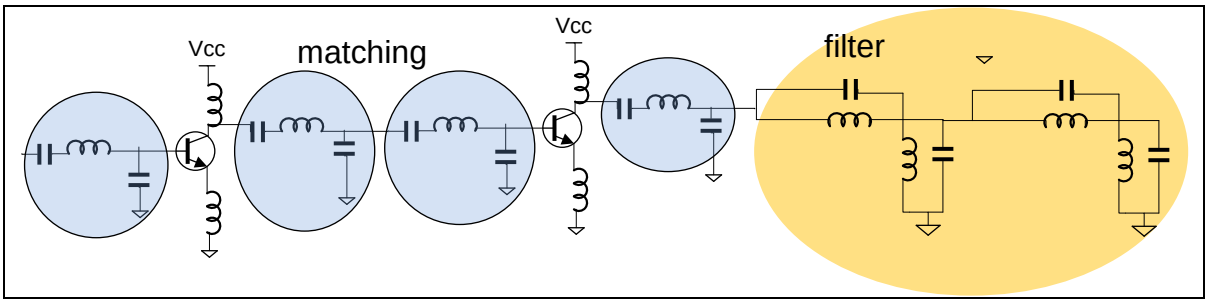

Figure 2. Matching Stages And Filters Cascading With Potential Waste

DesignAsyst™, depicted schematically in Figure 3 provides a comprehensive top-down A/M-S/RF communication design environment enabling users to rapidly trade off among subsystem/circuit specifications in order to achieve overall system performance specifications. Its analyses cover the entire link (symbols to symbols) and account for impairments such as channel and device noise, blockers and interferers and device nonlinearities. It provides efficient and accurate computation of system specifications such as Bit Error Rate [BER], Error Vector Magnitude [EVM], and Signal to Noise Ratio [SNR]. It provides design debugging tools such as Constellation Diagrams, Eye Diagrams and Frequency Spectra as shown also on Figure 3.

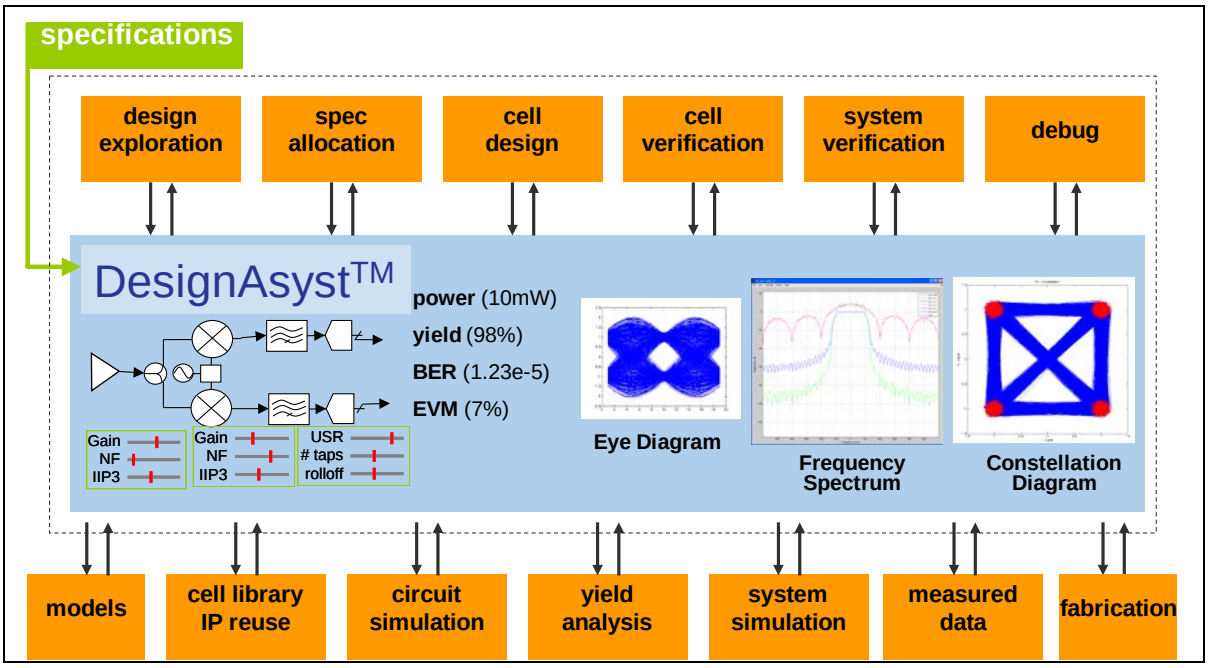

Figure 3. DesignAsyst™: A True Top-Down Design Methodology

DesignAsyst™ is architected so as to be able to work at the outset with proprietary macromodels of subsystem cells that can be tied via Process Design Kits [PDKs] directly to specific processes. These macromodels realistically depict tradeoffs among circuit parameters such as gain, noise figure [NF], third-order input intercept [IIP3], power consumption, etc. Using these it can compare among different topologies and compute yield/power tradeoff. In addition to its proprietary macromodels, DesignAsyst™ is architected ultimately to be able to accept circuit simulation data or even measurements better to inform accuracy at the system analysis level.

DesignAsyst™ is built on a proprietary analysis engine that efficiently accounts for the effects of impairments, such as nonlinearity and noise on the overall system specifications. Figure 4 shows a typical RF receiver comprised of a cascade connection of an LNA, Mixer, Voltage Controlled Oscillator [VCO], Amplifier and Analog to Digital Converter [ADC] as well as appropriate filters. Figure 6 shows the results of analyses of that receiver

in the presence of an interferer signal for various BERs. Because DesignAsyst™ is orders of magnitude more efficient computationally than conventional simulators (Figure 5), it can be employed for design studies heretofore impossible.

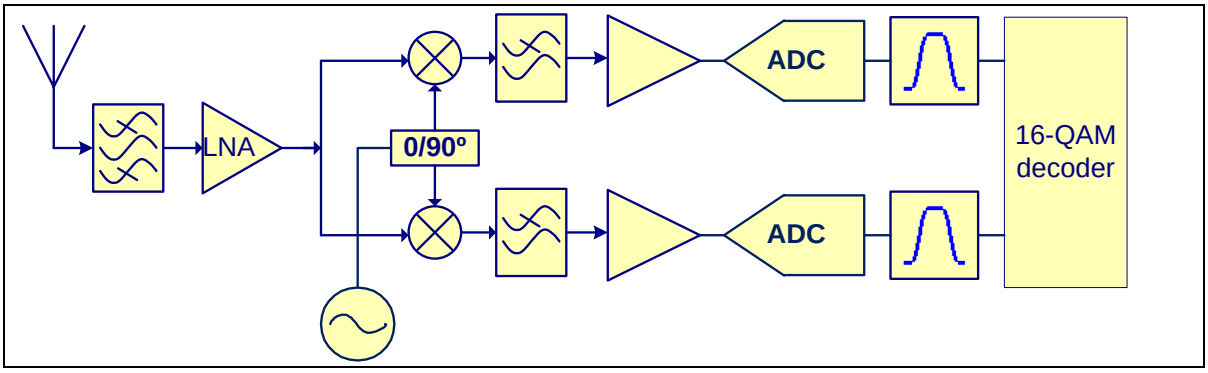

Figure 4. Generic 16-QAM direct-conversion receiver

Complex digitally generated signals defy traditional spreadsheet analysis. Analysis efficiency is extremely important for comprehensive design exploration. Complex communication and sensing systems require exhaustive coverage of their input signal spaces. Low BER systems may require computer-weeks of conventional simulation. Because of that, such simulation may be jettisoned in favor of expensive trial-and-error prototyping. Moreover, even such elaborate simulations may not provide design debugging insight.

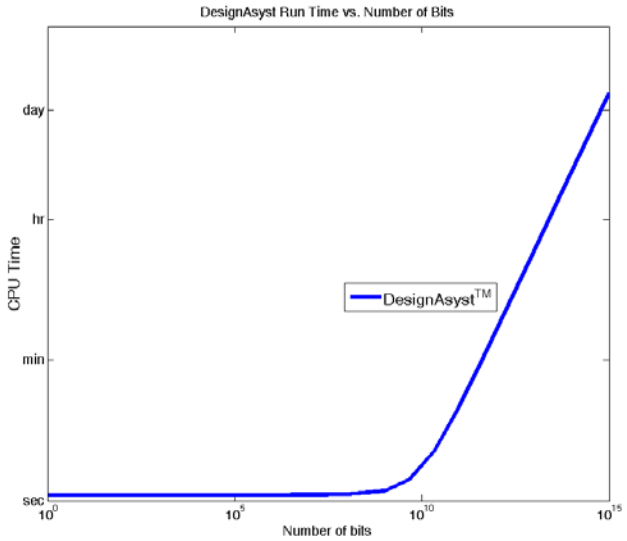

Figure 5. Bit Error Rate versus CPU time for DesignAsyst™

DesignAsyst™ features accurate modeling of impairments: multiple interferers and blockers; nonlinearity; noise; I/Q mismatch; phase noise. It encompasses continuous and discrete time system components being truly mixed-signal in nature: simultaneously addressing analog and digital components without employing time-consuming and expensive co-simulation schemes. The models are electrical, thereby enabling study of effects of inevitable mismatches among subsystem circuit components on overall system performance.

Using its proprietary macromodels for the subsystem cells, designers can do real time what-if analysis in terms of their parameters; e.g., gain, noise figure and nonlinearity as specified in terms of IIP2 and IIP3. Figure 6 shows examples of the impact of changes of such parameters on the BER of the example receiver. Additionally, various plots of interest, such as eye-diagram, constellation plot and frequency response can be displayed for diagnostic purposes as shown in Figure 3.

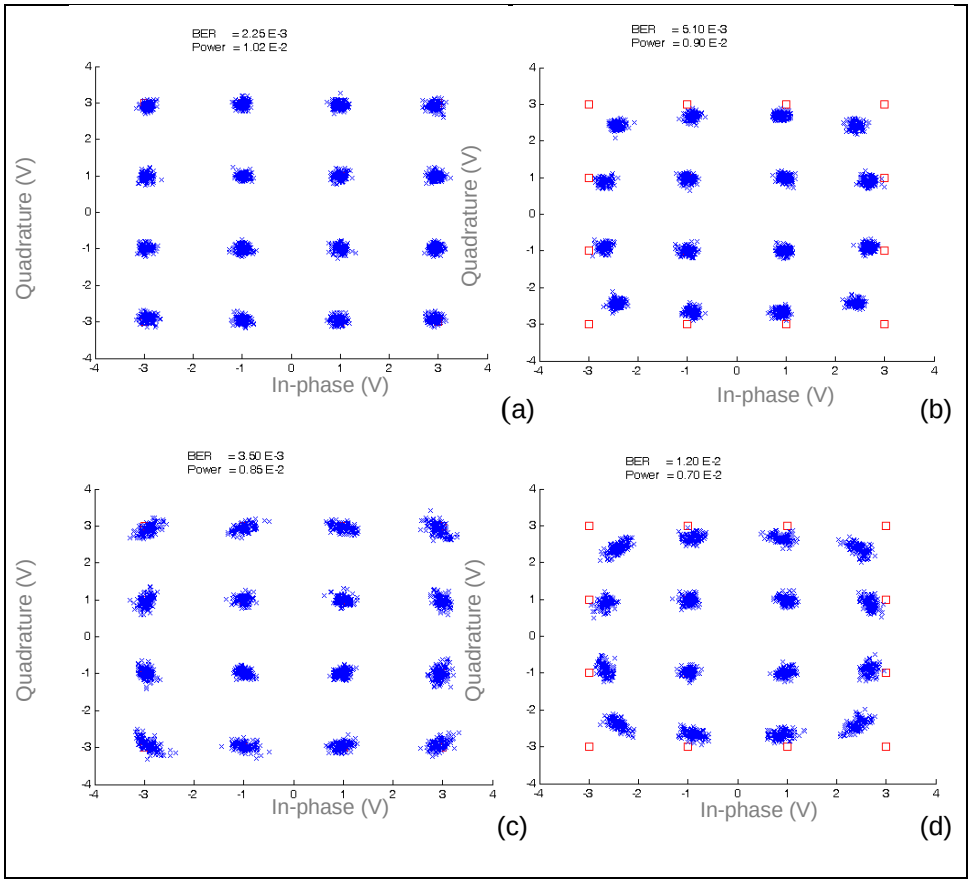

Figure 6. Constellation Diagrams.
Effects of various impairments: a) Additive White Gaussian Noise [AWGN] in the channel; (b) Higher nonlinearity leads to compression; c) Higher phase noise leads to smearing of the constellation; d) Combined effects of both high nonlinearity and high phase noise

DesignAsyst™ provides cell-level insight to system designers and system-level insight to cell designers, thereby improving communications among design team members. Such tight coupling among the team members greatly reduces design iterations while providing an extremely high probability of early silicon success. DesignAsyst™ computational efficiency enables extensive topological design exploration so as to be able to optimize for high yield and low power consumption at the system level.

The AFRL continues to seek better design solutions and that quest has led to this contract in support of the second phase of the MDREX program, MDREX II. It is widely known that developing EDA solutions for a design program under way is difficult in terms of synchronization and alignment of resources. For that reason, the systemIC effort requirements were informed by MDREX II goals but the schedules and executions were independent.

2.2 Project Objectives

The overall technical objectives of the project have been to research and develop a better system design methodology for mixed-signal integrated circuits and a design environment to support the methodology.

2.3 Methods, Assumptions, and Procedures

The program was organized into three distinct but interrelated technical tasks each of which was aimed at achieving one of the above three program objectives. The eight tasks were initially defined as follows:

Task 1: Construct Receiver Schematic and Testbenches: In this task, the schematics for the receiver, the cells that make up the receiver and the testbenches to measure the performance of the receiver were constructed in DesignAsyst™.

Task 2: Develop Macromodels: In this task, macromodels for each cell in the receiver were developed and tested.

Task 3: Develop Macromodel for an Analog to Digital Converter (ADC): In this task, a macromodel was developed for the analog to digital converter was developed. Although the ADC is not part of the receiver IC, it has significant impact on the performance of the radar and therefore was included in the analysis.

Task 4: Extend System Design Environment Analysis and Simulation Capabilities: In this task, several analysis, simulation and user interface modules were developed within DesignAsyst™ required for the test benches developed in Task 1.

Task 5: Design Space Exploration and Specification Allocation: In this task, software capabilities were developed to explore the design space offered by the architecture and the parameter ranges of the cells that make up the receiver. These capabilities assist the system designer to set specifications for the cell designs and for each set of specifications display the overall performance of the system.

Task 6: Research further opportunities in mixed-signal system design: In this task, we explored opportunities for further improving mixed-signal design capabilities for USAF and USAF contractor designers.

Task 7: Analysis Development: This task is a continuation of Task 4 and involves more advanced development of analysis, simulation and user interface capabilities.

Task 8: Receiver Design Demonstration: In this task, new capabilities of the design environment are demonstrated.

The task definitions evolved to best meet the overall project objective with the availability of information and resources and intermediate research results. These are detailed in Section 3.

2.4 Project Team

Ronald Rohrer, Aykut Dengi and Nagendran Rangan worked on this project. Ronald Rohrer is a world-renowned expert in simulation and design automation. Aykut Dengi has worked on electronic design automation for 20 years and has significant contributions to the design and analysis of analog, radio frequency and high performance digital circuits. He was a principal investigator in the DARPA NeoCAD program and led the UltraSYN team. Nagendran Rangan formerly is an experienced software engineer who worked on the UltraSYN team as well as the development of the DesignAsyst^{TM} capability.

3. Results and Discussion

The project balanced three threads: research and development of a novel design methodology; research and development of a novel design capability in support of this methodology; and the demonstration of the methodology and capability on a relevant design. The first section will describe the new design methodology developed and contrast it with existing design methodology. The second section will describe the novel mixed-signal system design capability including analysis, design exploration, specification allocation. The third section will present validation results.

3.1 Research and Development of a Novel Design Methodology

We have attempted to solve many of the issues in the traditional design methodology described above:

1. Separation of digital and analog portion[s] of a system
2. Fixed [pre-determined] impedance between components
3. Lack of accurate and parameterized macromodels for components
4. Severely limited design reuse
5. Lack of complete system simulation

Issues 1 and 5 are largely addressed in Section 3.2 below. In this section we will describe how we addressed issues 2-4.

Recognizing that hierarchy is indeed a critical part of system design and cannot be gainfully disposed of, we redefine the boundaries of such hierarchical decomposition. In each functional active component, such as an amplifier, we separate the active devices on the signal path that perform the function, and the passive devices that perform as loads and provide filtering and matching. There may be a few such active clusters in a component and those clusters also have functional definitions, such as a *transimpedance stage*. We call these clusters *mini-macros* (Figure 7). We then cluster the passives that remain, even across component boundaries, e.g., combining the output matching stage of an LNA, a filter, and the input matching stage of a mixer into one *passive macro* (Figure 7).

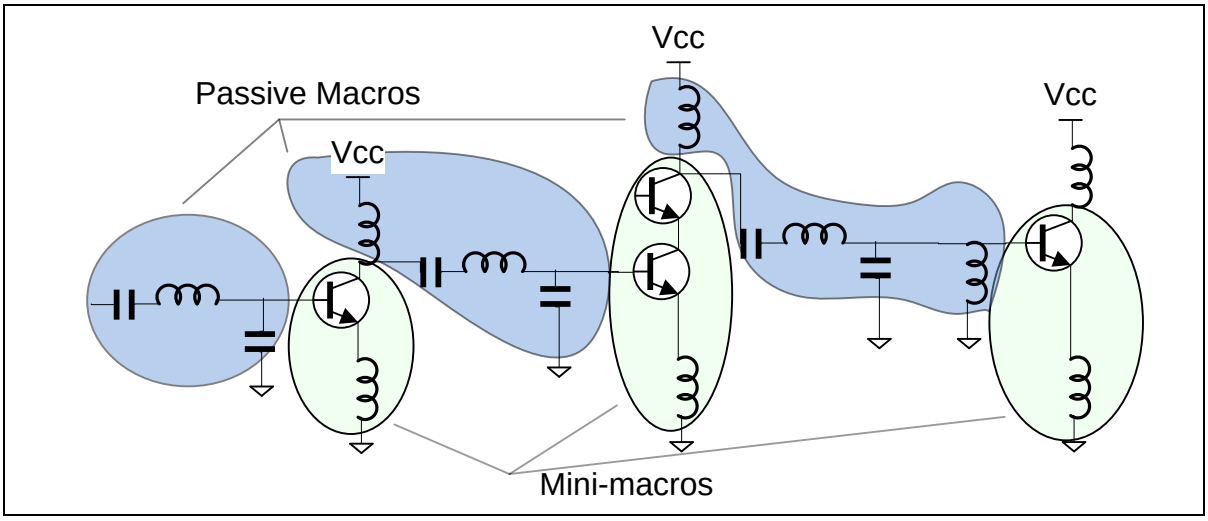

Figure 7. Passive Macros And Mini-Macros.
Passive Elements are clustered into *passive macros* and active device clusters into *mini-macros.*

The passive macro is then abstracted into an n-port circuit. We have developed a behavioral model for such passive macros that comprehend load, matching and filtering functions of the passives as abstract design goals. The matching can be to a fixed impedance but the most useful mode is the automatic match to active element inputs and outputs where a broadband match is obtained for the frequency-dependent complex impedances at the input and output over the specified frequency band of interest. Additionally, filtering specifications may be incorporated instead of merely seeking a flat response (0).

In addition to the matching and filtering goals, the system designer can specify the filter order and topology as design parameters. The passive macro is informed by of the non-idealities of the passive elements by the Process Design Kit (PDK), e.g., the quality factors of the inductors and the capacitors, etc. Hence the system designer is able to evaluate the performance of the system including all the impairments *in his top-down design*.

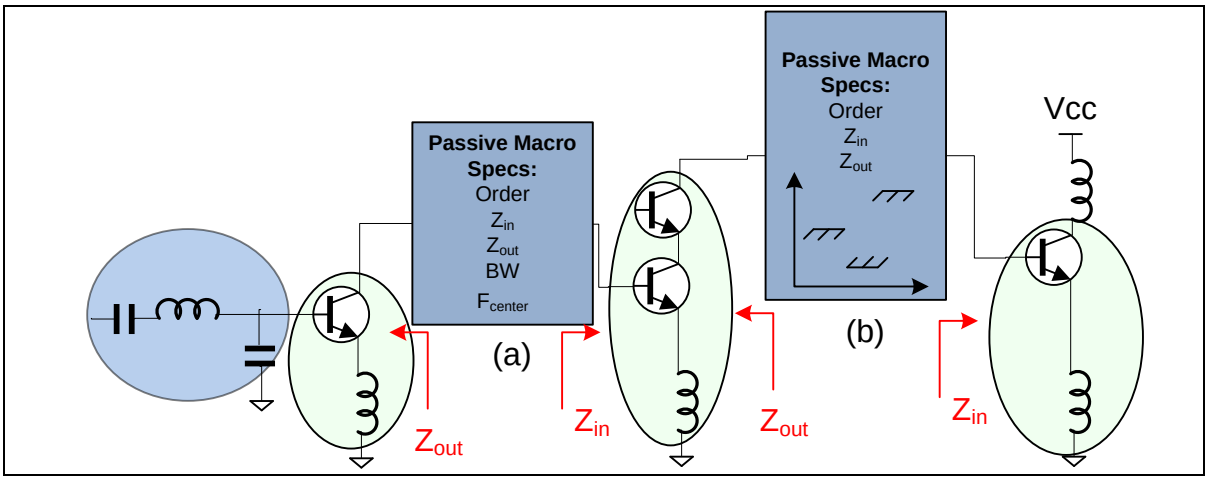

Figure 8. Passive Macro Configured For: (a) A Flat Match; (b) With Filtering. The *passive macro* in (a) specifies a flat match between to *mini macros* with centered at frequency F_{center} and with a bandwidth of BW. The *passive macro* in (b) specifies a match between to *mini macros* and filter passband and stopband specifications indicated on the graph.

A synthesis module that realizes the abstract passive macro in the target process was also developed. This realization is meant as a guide for the component designer and can be improved. Furthermore, this abstract model provides an excellent route for design reuse: the abstract model remains as a guide when the process has to be repeated if the specifications change or another process is targeted. We can contrast that to the reality today where an engineer finds it difficult to understand an earlier passive design and must start from scratch for each design iteration.

3.2 Research and Development of a Novel Design Capability

As discussed in Section 3.1, the design of integrated circuit mixed-signal systems relies heavily on design automation capability, in particular analysis and simulation. Several significant improvements were made to the DesignAsyst™ capability described above in Section 2.1 to address the needs of the USAF designers and to support the novel design methodology described in Section 3.1.

The following capabilities were added to DesignAsyst™ analysis capability.

1. Support for several devices from the IBM SiGe 8HP process design kit (the manufacturing process used for the MDREX project): bipolar transistor (BJT), spiral inductor, transmission line element (lossy and lossless)
2. Several behavioral models for top-down design: variable gain amplifier (VGA), diode mixer, analog to digital converter.
3. A generalized N-port s-parameter model to support measured data

4. A generalized filter element that accepts pass-band and stop-band specifications, in addition to the existing filter-type/order specifications.
5. Spectre netlist parsing (for reading MDREX circuit netlists)
6. Parameter sweep and display of sweep results, in particular for the Local Oscillator (LO) power sweep
7. Hierarchical simulation: see detailed discussion below
8. Transistor-level simulation: see detailed discussion below
9. Frequency planning and spur analysis
10. LINUX support: AFRL designers (and most integrated circuit designers elsewhere) use LINUX workstations. DesignAsyst™ was ported to LINUX for this reason. The make environment now supports both Windows and LINUX platforms.
11. Specification allocation feasibility GUI: see detailed discussion below
12. Optimization module: see detailed discussion bellow

Hierarchy is pervasive in design and is critical in managing complexity. Circuit simulation algorithms, however, have required flattening even if they allowed hierarchical inputs, which they flatten inside. The result is quickly deteriorating simulation speed with increasing circuit complexity. A true hierarchical simulation technology was developed in DesignAsyst™, which allows it to overcome the simulation capacity problems discussed above.

System designers often use experience in coming up with block specifications, but they may require a higher performance than is feasible on the target technology, especially if they do not have prior experience on that technology. The specification allocation feasibility GUI in DesignAsyst™ allows system designers to see feasible design points in a parallel coordinates chart (blue lines in 0) along with the specifications they have allocated (red line). The system designer is therefore aware of the quantitative risk in picking the particular set of specifications, i.e., if the specifications fall far from the feasible design points, it is likelier that the block designer would not be able to implement a circuit design that meets those allocated specifications.

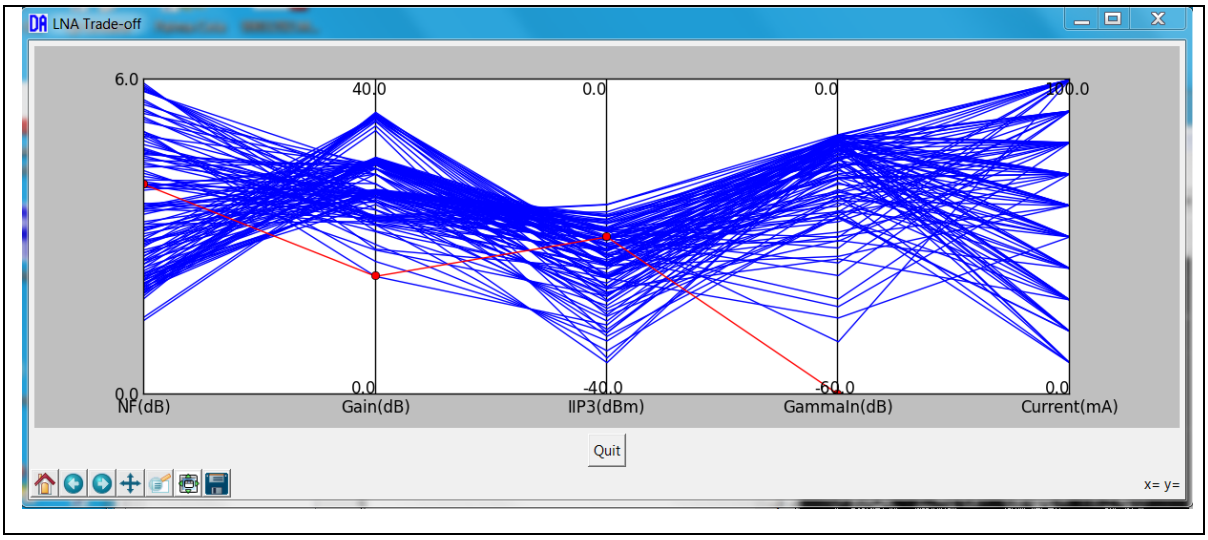

Figure 9. The Specification allocation feasibility GUI

One of the challenges in supporting the design methodology introduced in Section 3.1 is that nonlinearities presented by the active devices are not filtered by passive elements before they reach the ports of the macromodel. Therefore traditional macromodels are not sufficiently accurate, especially for verification of transistor-level block designs in a system setting. Co-simulation is too slow and inaccurate as well. To fill this void, a transistor-level simulation capability which is fully compatible with the DesignAsyst™ hierarchical analysis algorithm was developed. This simulation algorithm is completely different from SPICE and its many clones, which forms the basis of almost all simulation programs in the market. The transistor level simulation algorithm is at the prototype stage.

An optimization capability was implemented in DesignAsyst™ to help achieve a system design optimal in global system metrics, such as power consumption, while meeting all performance specifications. Although the capability is functional, it is not clear whether system designers are willing to use an automated capability.

3.3 Demonstration

The capabilities described above were demonstrated on the AFRL DREX receiver design [1] (0). Macromodels for the components of the receiver were derived. The system was analyzed using DesignAsyst™ and the results were compared to measurements. Specifically, RX1 (upconversion stage) gain predicted by DesignAsyst™ agreed with measurements over the frequency of interest (see 0). The Noise Figure and OIP3 for RX1 also agreed with the design goals (see Table 1).

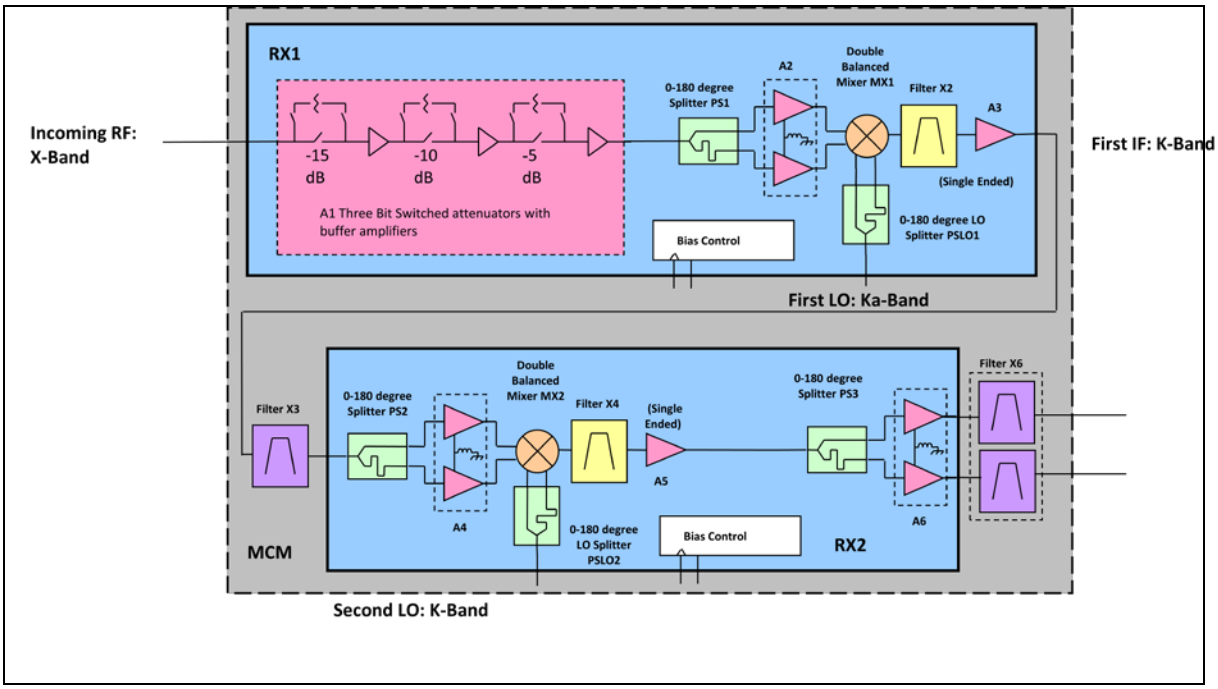

Figure 10. AFRL DREX Receiver Schematic

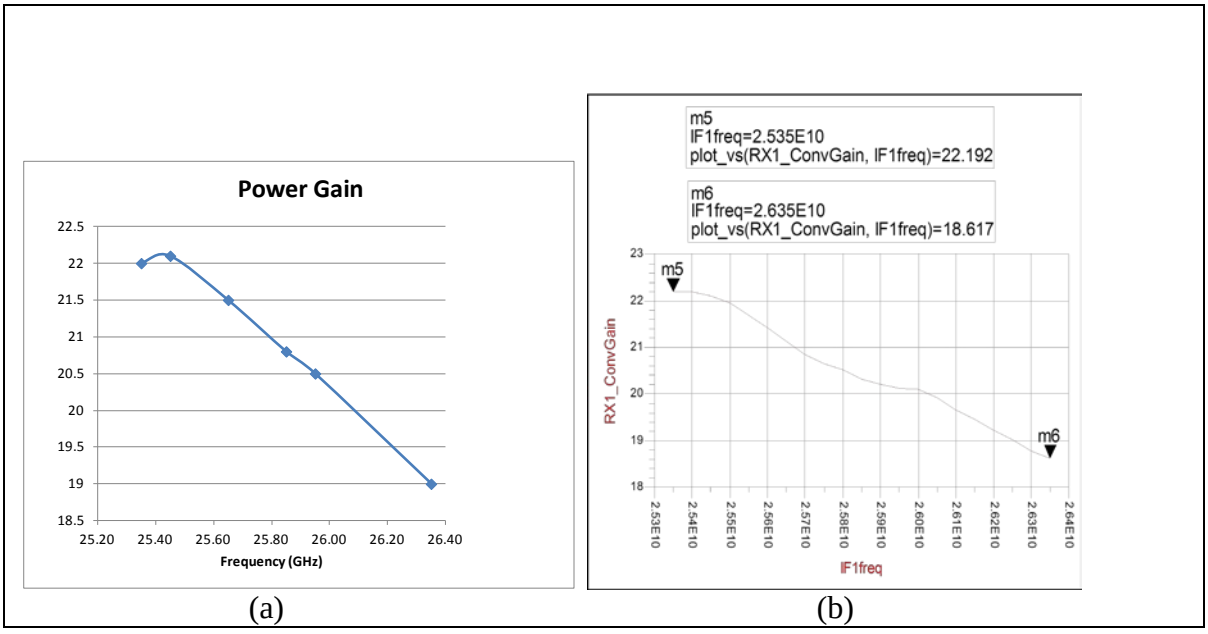

Figure 11. Gain of RX1 over frequency of interest (a) analysis vs. (b) measurement

Table 1. RX1 NF and OIP3 (analysis vs. goals)

Specification	Goal	Analysis
NF	< 5 dB	4.72 dB
OIP3 (Input @ 10GHz)	> 15 dBm	18.13 dBm

To demonstrate the design methodology for passive macros, the interface between a low noise amplifier (LNA) and a mixer was investigated. The original LNA was designed to match an output impedance of 50 Ohms. Similarly, the mixer input was matched to 50 Ohms. The passives between the LNA and the mixer were then consolidated per the methodology described in Section 3.1. The results are presented in Table 2 and 0.

Table 2. Comparison of Original and Consolidated Designs

	Original	Consolidated
Number of passives	19	5
Gain (dB)	39	39.5
NF (dB)	2.9	2.7

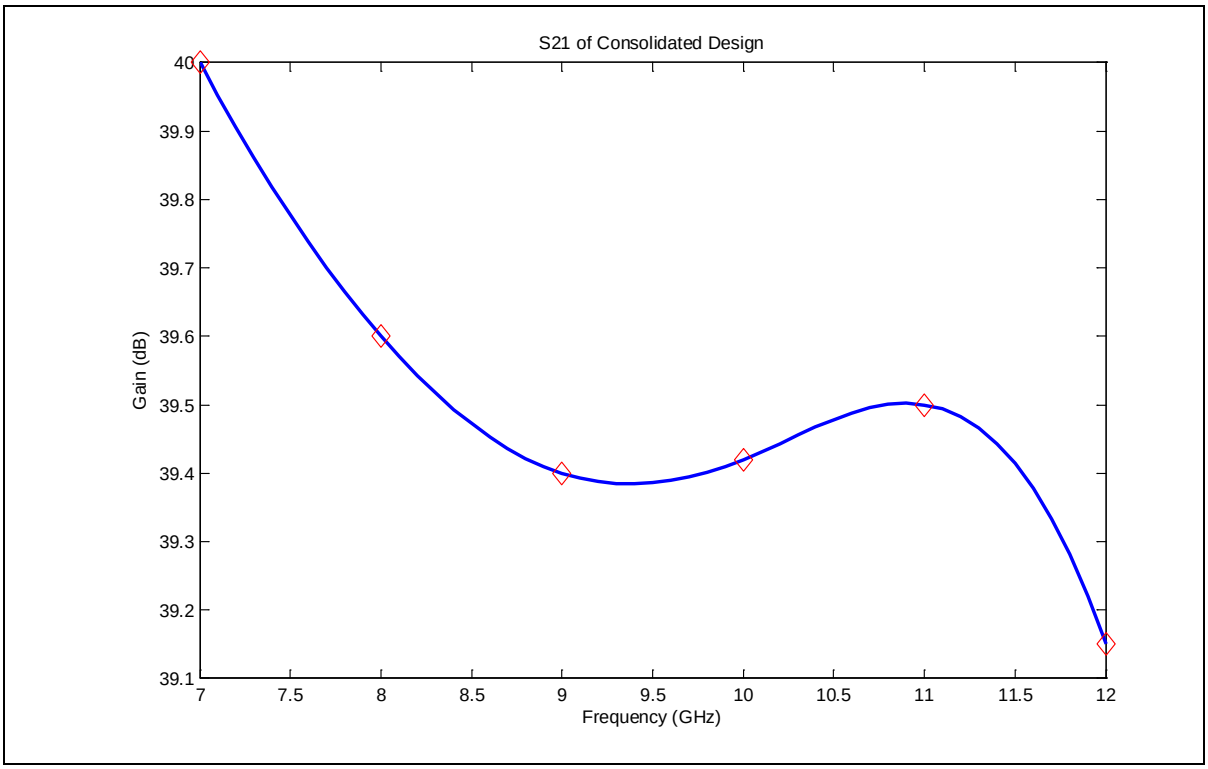

Figure 12. Frequency Response of Consolidated Design

4. Conclusions

This project has advanced significantly the state of the art in analog/mixed-signal/radio frequency integrated circuit system design methodology and its supporting design automation technology. The new design methodology offers important improvements in system performance as well as in system design productivity. The system performance gains are due to the ability to reduce redundancy and better adapt to rapidly evolving integrated circuit process technologies. The potential design productivity gains are due to improved re-use as well as the reduction in the number of iterations required to reach a superior system design. The novel analysis and simulation algorithms developed in this project have the potential to significantly impact performance of systems under design by allowing the analog and digital parts to be simultaneously optimized; by reducing the need for unnecessarily gross design margins by increasing the accuracy and prediction capability of the verification process; and by enabling the novel design methodology. Together, the methodology and design automation technology can help to reduce the non-recurring engineering costs and the cost-overruns that may arise in some USAF programs.

The feasibility of both the methodology and the algorithms has been demonstrated. Efforts to integrate the technologies into existing design flows by major EDA vendors have, however, failed. Major EDA vendors seem to have little motivation to meet the unique requirements of the USAF. They also prefer not to enable a potentially disruptive technology that could rival their existing capabilities.

5. Recommendations

The significant advances made in mixed-signal integrated circuit system design methodology design automation technology offers an opportunity for the USAF in particular and the Department of Defense in general to gain a significant edge in the design of complex defense systems. As mentioned in the Conclusions section, these capabilities must be integrated into a complete design system to be gainfully deployed, but major EDA vendors are not willing to participate in such a venture. It would take a non-negligible, but compared to the cost of electronic defense systems very small, amount of investment to build on the results to create a complete design system that designers at the USAF, the DoD and their contractors can use. We recommend that such a project be started.

6. References

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[2] “Widely Tunable SiGe MMIC-Based X-Band Receiver,” Johnson et al, GOMAC 2009

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List of Acronyms, Abbreviations, and Symbols

Acronym	Definition
ADC	Analog to Digital Converter
AFRL	The Air Force Research Laboratory
BER	Bit Error Rate
DoD	Department of Defense
EDA	Electronic Design Automation
EVM	Error Vector Magnitude
IIP	Intermodulation Intercept Point
GUI	Graphical User Interface
IIP3	Input Intercept Point Three
LNA	Low Noise Amplifier
NF	Noise Figure
MDREX	Multiple Digital Receiver Exciter
OIP3	Output Intercept Point Three
QAM	Quadrature Amplitude Modulation
SNR	Signal-to-Noise Ratio
USAF	United States Air Force
USR	Upsampling Ratio
VCO	Voltage Controlled Oscillator